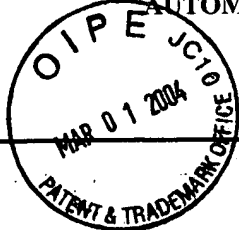


TRANSMITTAL OF FORMAL DRAWINGSDocket No.
BUR920030168US1 (17124)In Re Application Of: **Darren Anand, et al**

Serial No.	Filing Date	Confirmation No.	Examiner	Art Unit
10/707,071	November 19, 2003	Unknown	Unknown	Unknown

Invention: **AUTOMATIC BIT FAIL MAPPING FOR EMBEDDED MEMORIES WITH CLOCK MULTIPLIERS**Address to:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Transmitted herewith are:

8 sheets of formal drawing(s) for this application.

☒ Each sheet of drawing indicates the identifying indicia suggested in 37 CFR Section 1.84(c).
*Signature*Dated: **February 26, 2004****Steven Fischman**
Registration No. 34,594**Correspondence Address**
Customer No.: 23389I certify that this document and attached formal drawings
are being deposited on **2/26/04** with the
U.S. Postal Service as first class mail under 37 C.F.R. 1.8
and addressed to the Commissioner for Patents, P.O. Box
1450, Alexandria, VA 22313-1450.
*Signature of Person***Steven Fischman***Typed or Printed Name :*